A DISTRIBUTED, MEASUREMENT BASED, NONLINEAR MODEL OF FETs FOR HIGH FREQUENCIES APPLICATIONS

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ABSTRACT

For the first time, a FET nonlinear model, distributed along the gate length and extracted from pulsed I(V) and pulsed S-parameters measurements is presented. This model has led to a better prediction of power saturation mechanism and offers promising perspectives for intermodulation and nonlinear noise modeling at high microwave frequencies.

I - INTRODUCTION

The simulation and design of nonlinear microwave circuits require reliable large signal FET models. Today, two types of models are available : electrical models and physical models. On the one hand, no matter how accurate they are, physical models do not match with actual simulators due to the high computation power they need [1]. On the other hand, results given by electrical models are time efficient and quite reliable.

However, classical electrical equivalent circuit, based on a simple π topology, cannot take into account the channel distributed nature under the gate, which is very important for the prediction of large signal FET performances. Moreover, this model does not allow the inclusion of noise sources. It leads to a discrepancy between simulations and experimental data.

To address these problems, a new FET model based on a double π topology is presented. It allows a better representation of the global electrical performances as well as an insight of the intimate working of the transistor.

It provides also a straightforward way for the inclusion of noise sources.

First of all, the small signal equivalent circuit is described and explained. Secondly, the new nonlinear model is presented. Finally in order to verify the accuracy of our model, active load-pull measurements have been performed and compared with simulation results of distributed and classical models. An intermodulation simulation demonstrates an improved precision of our model on the classical one and opens promising perspectives in the field of noise electrical modeling for CAD.

II - SMALL-SIGNAL MODEL [2]

The key point of our approach for modeling FET is to consider the region under the gate like an active transmission line [3]. The resistor of each cell of the active line is substituted by a voltage controlled current generator and its associated conductance wired up in parallel. The choice of the number of cells to consider is justified by the achievement of a trade off between the minimum cells needed for an accurate distributed representation of the channel under the gate and the maximum cells allowing an easy and fast extraction. Two cells give a realistic description of the FETs. The three capacitances, C1, C2 and C3 of the active transmission line constitute a distributed capacitance all along the conductor channel. They represent the depleted region. A fourth capacitor C4 is included to model the electrostatic coupling between the two different areas highly doped under source and drain contacts and some distributed effects in the channel. To take into account the non instantaneous response of both current sources, with respect to the Vgs control voltage, a time delay is added to each transconductance : $gm_i = gm_{oi} e^{j\omega\tau_i}$ (i=1,2).

The extrinsic elements Rg, Lg, Rs, Ls, Rd and Ld have exactly the same topology and values as in the classical model. They are extracted by an optimization method presented in [4].

The resultant topology is represented figure 1

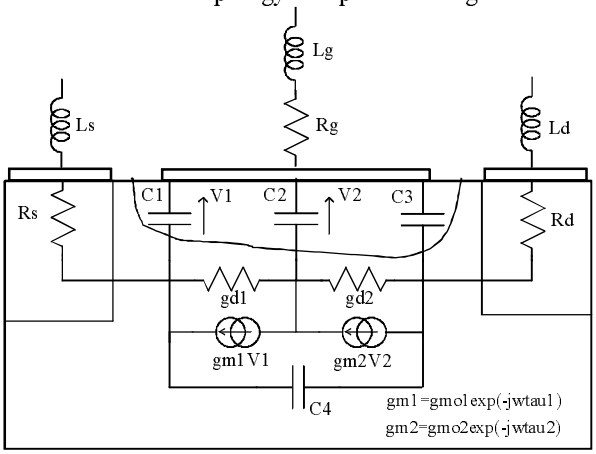

figure 1: Small signal distributed equivalent circuit.

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The intrinsic Y-parameters expressions are :

$$Y_{11} = j\omega C_1 + j\omega C_3 + j\omega C_2 \frac{gd_1 + gd_2 + gm_1}{gd_1 + gd_2 + gm_2 + j\omega C_2}$$

$$Y_{12} = -j\omega C_3 - j\omega C_2 \frac{gd_2}{gd_1 + gd_2 + gm_2 + j\omega C_2}$$

$$Y_{21} = -j\omega C_3 + \frac{gd_1 gm_2 + gm_1(gm_2 + gd_2) - j\omega C_2 gd_2}{gd_1 + gd_2 + gm_2 + j\omega C_2}$$

$$Y_{22} = j\omega C_3 + j\omega C_4 + \frac{gd_2(gd_1 + j\omega C_2)}{gd_1 + gd_2 + gm_2 + j\omega C_2}$$

The intrinsic model elements C1, C2, C3, C4, τ_1 and τ_2 are extracted using an optimization on the intrinsic Y-parameters for all bias points. So that, gm1, gm2, gd1 and gd2 values are fixed from the I(V) derivatives. Figure 3 shows the C1, C2, C3 and C4 evolution with Vgs voltage.

III - THE NONLINEAR DISTRIBUTED MODEL

The nonlinear modeling process was started by identifying the various elements of the model which are known to have weak bias dependence. C2, C3, C4, τ_1 and τ_2 are specified linear and fixed to their small signal average value. In addition to the two current generators, we found C1 depending on the bias, according to figure 3. Thanks to the double π topology, the gate conduction modeling can be distributed. All these nonlinearities are extracted from pulsed I(V) and pulsed S-parameters measurements.

Figure 2 presents the large signal nonlinear model :

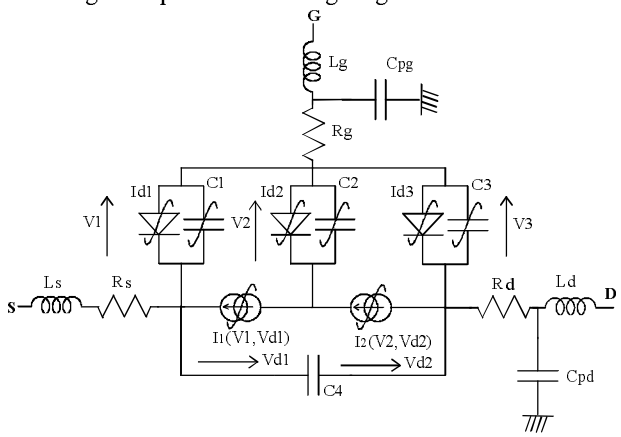

Figure 2 : The nonlinear distributed model.

The drain current modeling is performed using two current generators controlled by four different voltages. I_1 is controlled by the voltage drop (V1) between the gate and the source, and by its own voltage (Vd1). I_2 is controlled by the voltage drop (V2) between the gate and the point of the channel corresponding to the transition between I_1 an I_2 and by its own voltage (Vd2). Both currents are described with the model explained in [5]. The parameters of this equation are exactly the same for I_1 and I_2. Their values are extracted from an optimization on the pulsed I(V) measurements. This optimization needs algorithms based on simulated annealing. It is important to notice that for an usual DC working (no gate conduction and no breakdown) the drain current is only performed by I_1 and I_2 connected in series. Thus, both sources must provide the same current although their commands are different. Figure 4 shows a comparison between simulated and measured I(V) characteristics, illustrating the very good fit.

Figure 5 shows the good agreement obtained between measured and computed S parameters at the bias point. Moreover, the values obtained for the elements of the equivalent circuit are given table 1. It should be noticed that the high values of the self inductances Lg and Ld are due to the bonding wires of the device.

The bias dependence of the capacitances is described with an analytical expression. For sake of simplicity, only the dependence of C1 with its own voltage (V1) has been taken into account in the large-signal model.

The new equivalent circuit allows us to model the distributed gate current including a diode in parallel with everyone of the depletion channel region associated capacitances. Each diode is represented with the classical expression : $I_{di} = I_s e^{\alpha V}$. I_s and α have the same value for I_{d1}, I_{d2} and I_{d3}. They are controlled by their own voltage drop. The three diodes provide gate current for high conductive Vgs. Note that, the gate current is more important near the source than near the drain, which is closed to the physical phenomena.

IV - MEASUREMENTS AND MODEL ACCURACY

In order to verify the accuracy of the new model, load-pull measurements [6] have been performed. They are compared with simulation results of distributed and classical model.

Power transfer characteristics of a 0.5*1200 μm^2 HFET have been determined at 10 GHz for an optimum load impedance of 14.42+j*1.92 Ω. The device was biased at Vds = 9 V and Vgs = -2.9 V. The aim of the simulations presented figures 6 ,7 and 8 is to demonstrate the accuracy of our model for a nonlinear and compressed working at high frequencies. The double π model gives a more realistic output power than the simple π model. The improvement came from an early compression of the distributed equivalent circuit, which is close to the experimental data. This is explained by the fact that the drain current of the distributed model is controlled by a set of distributed voltage, V1 and V2. The last one is an internal voltage and allows a physical representation of the drain current's command process.

Note that, the remaining difference between simulation and measurement should be obliterated if thermal effects are taken into account.

The intermodulation simulation have been performed for two input frequencies f1 = 9.99 GHz and f2 = 10.01 GHz. Figure 9 represents the f1 and 2f1-f2 output power ratio (C/I) for both models. The result given by the distributed model shows significant differences in the IMD prediction at the onset of saturation. Preliminary measurements on the same device have demonstrated a peak in the C/I at an input power of 15 dBm which is better predicted by the distributed model than the classical one. More investigations are under progress. Because the double π topology includes an internal node, the frequencies mixing phenomena is better modeled in the distributed model. Theses results open interesting perspectives in the fields of noise simulations [7].

V - CONCLUSION

A new distributed large signal model for FET and HEMT based on a double π topology has been presented. The equivalent circuit represents a more realistic electric topology close to the main physical phenomena which determine the device behavior. Load pull measurements and intermodulation simulations have been performed. They show a very good accuracy of our model over the classical model. It provides also a natural way for the inclusion of noise sources.

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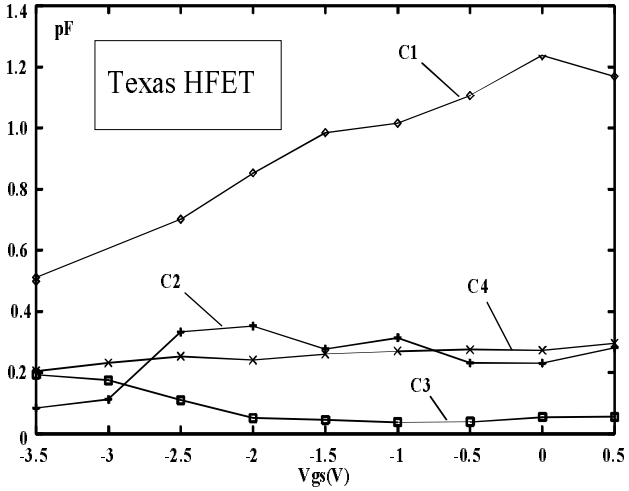

figure 3 : Bias dependence of C1, C2, C3 and C4 with Vgs.

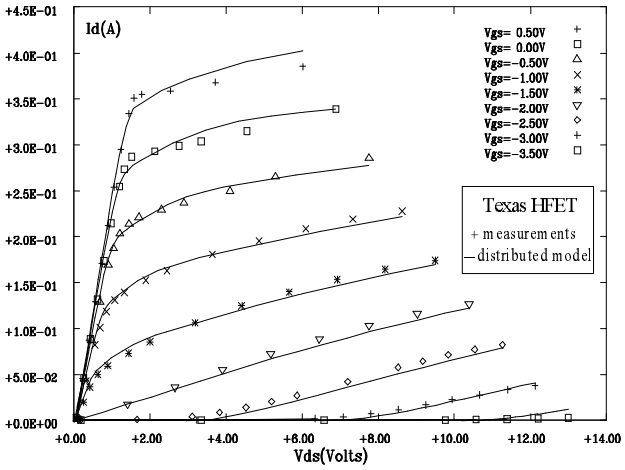

Figure 4 : Measured and modeled pulsed I-V characteristics of the HFET transistor.

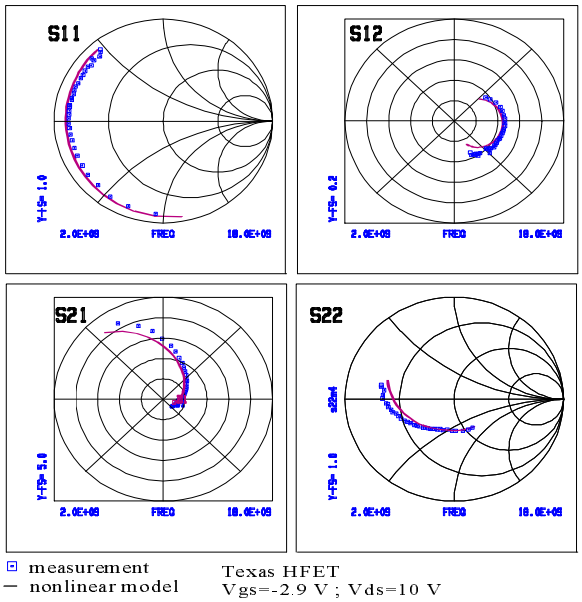

figure 5 : Comparison between pulsed S-parameters measurements and nonlinear distributed model.

Rg=0.4 Ω	Rd=0.8 Ω	Rs=0.8 Ω
Lg=265 pF	Ld=245 pF	Ls=9 pF
C1=670 fF	C2=205 fF	C3=45 fF
C4=250 fF	τ1=0 ps	τ2=1 ps
Gm1=99 mS	Gd1=48 mS	Gm2=62 mS
Gd2=34 mS	Cpg=45 fF	Cpd=30 fF

table 1 : Values of the small signal model elements (Vds=9V Vgs=-2.9 V)

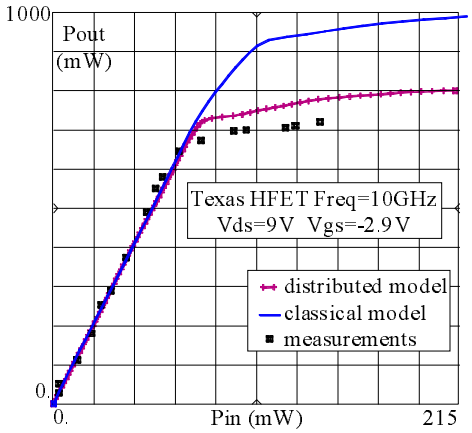

figure 6 : Measured and simulated output power using distributed and classical model.

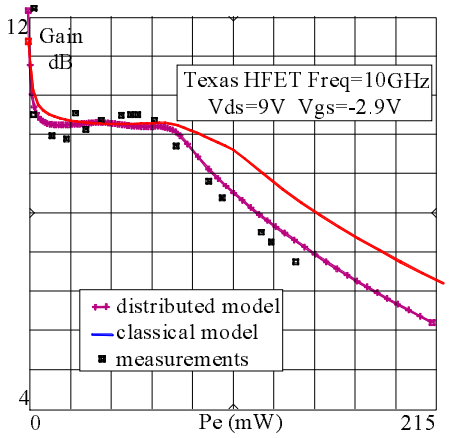

figure 7 : Measured and simulated Gain using distributed and classical model.

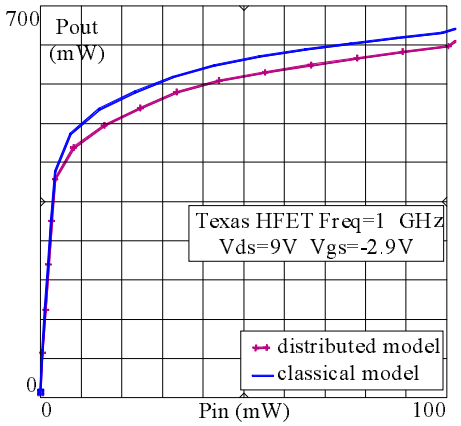

figure 8 : Output power simulated using classical and distributed model.

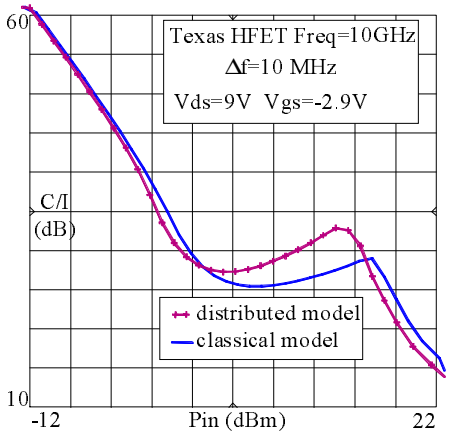

figure 9 : C/I simulated using classical and distributed model.